TEXAS INSTRUMENTS

PCM5100A, PCM5101A, PCM5102A
PCM5100A-Q1, PCM5101A-Q1, PCM5102A-Q1

SLAS859B – MAY 2012 – REVISED FEBRUARY 2015

PCM510xA 2.1 V_{RMS} DirectPath™, 112/106/100 dB Audio Stereo DAC with PLL and 32-bit, 384 kHz PCM Interface

1 Features

- Qualified in accordance with AEC-Q100
- Direct Line Level 2.1VRMS output
- Ultra Low Out-of-Band Noise
- No DC Blocking Capacitors Required
- Intelligent Muting System; Soft Up or Down Ramp and Analog Mute For 120dB Mute SNR
- Integrated High-Performance Audio PLL With BCK Reference To Generate SCK Internally
- Small 20-pin TSSOP Package
- Accepts 16-, 24-, And 32-Bit Audio Data
- PCM Data Formats: I^2S, Left-Justified
- Automatic Power-Save Mode When LRCK And BCK Are Deactivated.
- 1.8 V or 3.3 V Failsafe LVCMOS Digital Inputs
- Hardware Configuration
- Single Supply Operation:
  - 3.3V Analog, 1.8 V or 3.3 V Digital

2 Applications

- A/V Receivers, DVD, BD Players
- Automotive Infotainment and Telematics
- HDTV Receivers

3 Description

The PCM510xA devices are a family of monolithic CMOS integrated circuits that include a stereo digital-to-analog converter and additional support circuitry in a small TSSOP package. The PCM510xA uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

Using Directpath™ charge-pump technology, the PCM510xA provides 2.1 V_{RMS} ground centered outputs, allowing designers to eliminate DC blocking capacitors on the output, as well as external muting circuits traditionally associated with single supply line drivers.

The integrated line driver surpasses all other charge-pump based line drivers by supporting loads down to 1 kΩ.

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock), allowing a 3-wire I^2S connection and reducing system EMI.

Intelligent clock error and PowerSense under voltage protection utilizes a two level mute system for pop-free performance.

Compared with many conventional switched capacitor DAC architectures, the PCM510xA family offers up to 20 dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100 kHz OBN measurements all the way to 3 MHz)

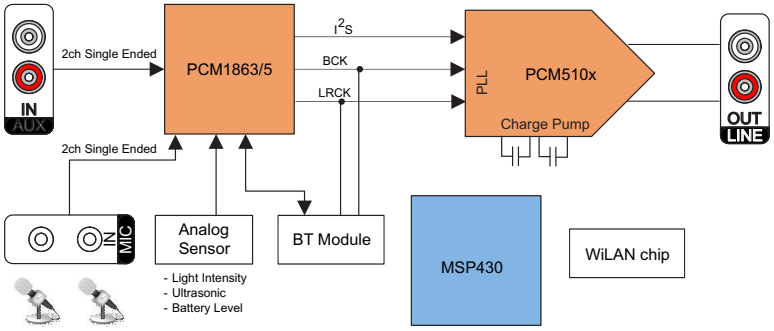
A block diagram for the product family can be found in *Functional Block Diagram*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM5102	TSSOP (20)	5.50mm × 4.40mm
PCM5101		
PCM5100		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified System Diagram



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2012) to Revision B — **Page**

- Added *ESD Rating* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* ... 1
- Added items to show 1.8V DVDD capability ... 1
- Changed the *Features* list. ... 1
- Changed "Operating Temperature Range " to "Operating Junction Temperature Range " ... 5
- Deleted redundant PLL specification ... 5
- Deleted "Intelligent clock error and ", "... for pop-free performance" ... 13
- Clarified clock generation explanation ... 24
- Clarified external SCK discussion. ... 25
- Deleted "The PCM510xA disables the internal PLL when an external SCK is supplied;" ... 25

Changes from Revision Initial (May 2012) to Revision A — **Page**

- Changed layout of first two pages ... 1
- Changed "VOUT = -1 dB" to " -1 dBFS" in THD+N ... 7
- Changed reference to correct footnote ... 9
- Changed t_{SCKH} and t_{SCKL} values to 9ns ... 10
- Removed 48kHz sample rate with PLL-generated clock ... 25

6 Device Comparison

Differences Between PCM510xA Devices

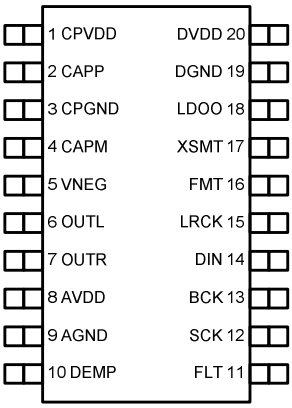
Part Number	Dynamic Range	SNR	THD
PCM5102A	112dB	112dB	–93dB
PCM5101A	106dB	106dB	–92dB
PCM5100A	100dB	100dB	–90dB

Typical Performance (3.3 V Power Supply)

PARAMETER	PCM5102/ PCM5101 / PCM5100
SNR	112 / 100dB
Dynamic Range	112 / 100dB
THD+N at - 1dBFS	–93dB
Full Scale Differential Output	$4.2V_{RMS}$ (GND center)
Normal 8× Oversampling Digital Filter Latency: $20t_S$	
Low Latency 8× Oversampling Digital Filter Latency: $3.5t_S$	
Sampling Frequency	8kHz to 384kHz
System Clock Multiples (f_{SCK}): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz	

7 Pin Configuration and Functions

PW 20-Pin Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CPVDD	1	—	Charge pump power supply, 3.3V
CAPP	2	O	Charge pump flying capacitor terminal for positive rail
CPGND	3	—	Charge pump ground
CAPM	4	O	Charge pump flying capacitor terminal for negative rail
VNEG	5	O	Negative charge pump rail terminal for decoupling, -3.3V
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
AVDD	8	-—	Analog power supply, 3.3V
AGND	9	—	Analog ground
DEMP	10	I	De-emphasis control for 44.1kHz sampling rate(1): Off (Low) / On (High)
FLT	11	I	Filter select : Normal latency (Low) / Low latency (High)
SCK	12	I	System clock input(1)
BCK	13	I	Audio data bit clock input(1)
DIN	14	I	Audio data input(1)
LRCK	15	I	Audio data word clock input(1)
FMT	16	I	Audio format selection : I^2S (Low) / Left justified (High)
XSMT	17	I	Soft mute control(1): Soft mute (Low) / soft un-mute (High)
LDOO	18	—	Internal logic supply rail terminal for decoupling, or external 1.8V supply terminal
DGND	19	—	Digital ground
DVDD	20	—	Digital power supply, 1.8V or 3.3V

(1) Failsafe LVCMOS Schmitt trigger input

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage	AVDD, CPVDD, DVDD	–0.3	3.9	V
	LDOO wtih DVDD at 1.8V	–0.3	2.25	
Digital Input Voltage	DVDD at 1.8V	–0.3	2.25	
	DVDD at 3.3V	–0.3	3.9	
Analog Input Voltage		–0.3	3.9	
Storage Temperature, T_{stg}		–40	85	°C
Storage Temperature, T_{stg}	Q1 devices	–40	125	

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
AVDD	Analog power supply voltage range	Referenced to AGND (1)	VCOM mode	3.0	3.3	3.46	V
			VREF mode	3.2	3.3	3.46	
DVDD	Digital power supply voltage range	Referenced to DGND (1)	1.8V DVDD	1.65	1.8	1.95	V
			3.3V DVDD	3.1	3.3	3.46	
CPVDD	Charge pump supply voltage range	Referenced to CPGND (1)		3.1	3.3	3.46	V
MCLK	Master Clock Frequency					50	MHz
LOL, LOR	Stereo line output load resistance			2	10		kΩ
C_{Lout}	Digital output load capacitance				10		pF
T_J	Operating Junction Temperature Range			–25		85	°C

(1) All grounds on board are tied together; they must not differ in voltage by more than 0.2V max, for any combination of ground signals.

8.4 Thermal Information

THERMAL METRIC (1)		PW	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	42.0	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	41.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
Data Format (PCM Mode)						
	Audio data bit length		16	24	32	Bits
f_S (1)	Sampling frequency		8		384	kHz
f_{SCK}	System clock frequency	Clock multiples: 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072			50	MHz
Digital Input/Output for non-Q1 devices						
	Logic Family: 3.3V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –4mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 4mA			0.22×DV_{DD}	
	Logic Family 1.8V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –2mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 2mA			0.22×DV_{DD}	
Digital Input/Output for Q1 devices						
	Logic Family: 3.3V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –4mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 4mA			0.22×DV_{DD}	
	Logic Family 1.8V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –2mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 2mA			0.3×DV_{DD}	

(1) One sample time si defined as the reciprocal of the sampling frequency. 1t_S = 1/f_S

Electrical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dynamic Performance (PCM Mode)(2)(3)							
	THD+N at –1 dBFS(3)	f_S = 48kHz	PCM5102		–93	-83	dB
			PCM5101		–92	–82	
			PCM5100		–90	–80	
		f_S = 96kHz	PCM5102		–93		
			PCM5101		–92		
			PCM5100		–90		
		f_S = 192kHz	PCM5102		–93		
			PCM5101		–92		
			PCM5100		–90		
	Dynamic range(3)	EIAJ, A-weighted, f_S = 48kHz	PCM5102	106	112		
			PCM5101	100	106		
			PCM5100	95	100		
		EIAJ, A-weighted, f_S = 96kHz	PCM5102		112		
			PCM5101		106		
			PCM5100		100		
		EIAJ, A-weighted, f_S = 192kHz	PCM5102		112		
			PCM5101		106		
			PCM5100		100		
	Signal-to-noise ratio(3)	EIAJ, A-weighted, f_S = 48kHz	PCM5102		112		
			PCM5101		106		
			PCM5100		100		
		EIAJ, A-weighted, f_S = 96kHz	PCM5102		112		
			PCM5101		106		
			PCM5100		100		
		EIAJ, A-weighted, f_S = 192kHz	PCM5102		112		
			PCM5101		106		
			PCM5100		100		
	Signal to noise ratio with analog mute(3)(4)	EIAJ, A-weighted, f_S = 48kHz		113	123		
		EIAJ, A-weighted, f_S = 96kHz			123		
		EIAJ, A-weighted, f_S = 192kHz			123		
	Channel Separation	f_S = 48 kHz	PCM5102	100	109		
			PCM5101	95	103		
			PCM5100	90	97		
		f_S = 96kHz	PCM5102		109		
			PCM5101		103		
			PCM5100		97		
		f_S = 192kHz	PCM5102		109		
			PCM5101		103		
			PCM5100		97		

(2) Filter condition: THD+N: 20Hz HPF, 20kHz AES17 LPF Dynamic range: 20Hz HPF, 20kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20Hz HPF, 20kHz AES17 LPF, A-weighted Channel separation: 20Hz HPF, 20kHz AES17 LPF Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the RMS mode.
(3) Output load is 10kΩ, with 470Ω output resistor and a 2.2nF shunt capacitor (see recommended output filter).
(4) Assert XSMT or both L-ch and R-ch PCM data are BPZ

Electrical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
	Output voltage			2.1		V_{RMS}
	Gain error		–6	±2	6	% of FSR
	Gain error on Q1 Devices		–7	±2	7	% of FSR
	Gain mismatch, channel-to-channel		–6	±2	6	% of FSR
	Gain mismatch, channel-to-channel on Q1 Devices		–6	±2	6	% of FSR
	PCM5100/1 Bipolar zero error	At bipolar zero	–5	±1	5	mV
	PCM5102 Bipolar zero error	At bipolar zero	–2	±1	2	mV
	Load impedance		1			kΩ
Filter Characteristics–1: Normal						
	Pass band				0.45f_S	
	Stop band		0.55f_S			
	Stop band attenuation		–60			dB
	Pass-band ripple				±0.02	dB
	Delay time			20t_S		s
Filter Characteristics–2: Low Latency						
	Pass band				0.47f_S	
	Stop band		0.55f_S			
	Stop band attenuation		–52			dB
	Pass-band ripple				±0.0001	dB
	Delay time			3.5t_S		s
Power Supply Requirements						
DV_{DD}	Digital supply voltage	Target DV_{DD} = 1.8V	1.65	1.8	1.95	VDC
DV_{DD}	Digital supply voltage	Target DV_{DD} = 3.3V	3	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3	3.3	3.6	VDC
CPV_{DD}	Charge-pump suply voltage		3	3.3	3.6	VDC
I_{DD}	DV_{DD} supply current at 1.8V(5)	f_S = 48kHz		7		mA
		f_S = 96kHz		8		mA
		f_S = 192kHz		9		mA
I_{DD}	DV_{DD} supply current at 1.8V(6)	f_S = 48kHz		7		mA
		f_S = 96kHz		8		mA
		f_S = 192kHz		9		mA
I_{DD}	DV_{DD} supply current at 1.8V(7)			0.3		mA
I_{DD}	DV_{DD} supply current at 3.3V(5)	f_S = 48kHz		7	12	mA
		f_S = 96kHz		8		mA
		f_S = 192kHz		9		mA
I_{DD}	DV_{DD} supply current at 3.3V(6)	f_S = 48kHz		8	13	mA
		f_S = 96kHz		9		mA
		f_S = 192kHz		10		mA
I_{DD}	DV_{DD} supply current at 3.3V(7)			0.5	0.8	mA
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(5)	f_S = 48kHz		11	16	mA
		f_S = 96kHz		11		mA
		f_S = 192kHz		11		mA
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(6)	f_S = 48kHz		22	32	mA
		f_S = 96kHz		22		mA
		f_S = 192kHz		22		mA

(5) Input is Bipolar Zero data.
(6) Input is 1kHz -1dBFS data
(7) Power Down Mode

Electrical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(7)	f_S = n/a		0.2	0.4	mA
	Power Dissipation, DV_{DD} = 1.8V(5)	f_S = 48kHz		48.9	185	mW
		f_S = 96kHz		50.7		
		f_S = 192kHz		52.5		
	Power Dissipation, DV_{DD} = 1.8V(6)	f_S = 48kHz		85.2	187	mW
		f_S = 96kHz		87		
		f_S = 192kHz		88.8		
	Power Dissipation, DV_{DD} = 1.8V(7)	f_S = n/a (Power Down Mode)		1.2		mW
	Power Dissipation, DV_{DD} = 3.3V(5)	f_S = 48kHz		59.4	92.4	mW
		f_S = 96kHz		62.7		
		f_S = 192kHz		66		
	Power Dissipation, DV_{DD} = 3.3V(6)	f_S = 48kHz		99	148.5	mW
		f_S = 96kHz		102.3		
		f_S = 192kHz		105.6		
	Power Dissipation, DV_{DD} = 3.3V(7)	f_S = n/a (Power Down Mode)		2.3	4	mW

8.6 Timing Requirements

Figure 1 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise.

			MIN	TYP	MAX	UNIT
t_{SCY}	System clock pulse cycle time		20		1000	ns
t_{SCKH}	System clock pulse width, High	DVDD = 1.8V	8			ns
		DVDD = 3.3V	9			
t_{SCKL}	System clock pulse width, Low	DVDD = 1.8V	8			ns
		DVDD = 3.3V	9			

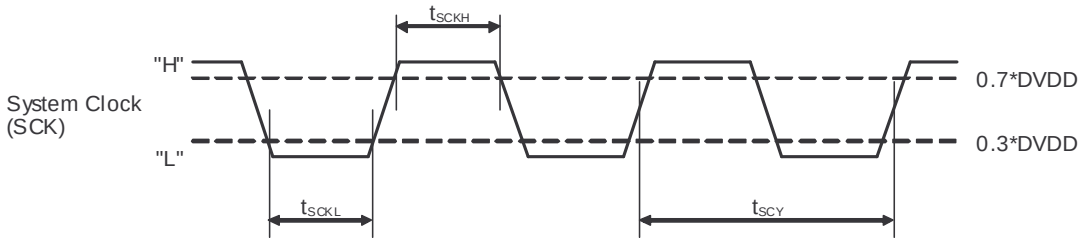


Figure 1. Timing Requirements for SCK Input

8.7 Timing Requirements, XSMT

		MIN	TYP	MAX	UNIT
t_r	Rise time			20	ns
t_f	Fall time			20	ns

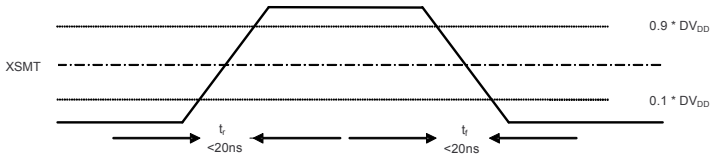


Figure 2. XSMT Timing for Soft Mute and Soft Un-Mute

8.8 Typical Characteristics

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

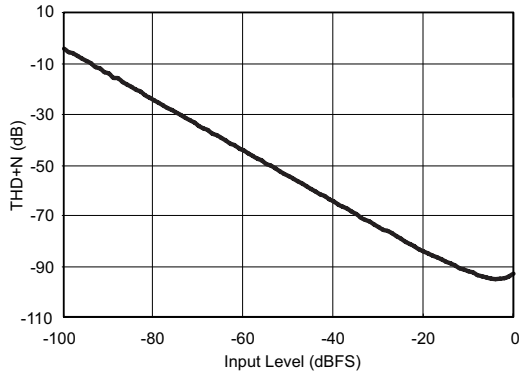


Figure 3. 1 THD+N versus Input Level

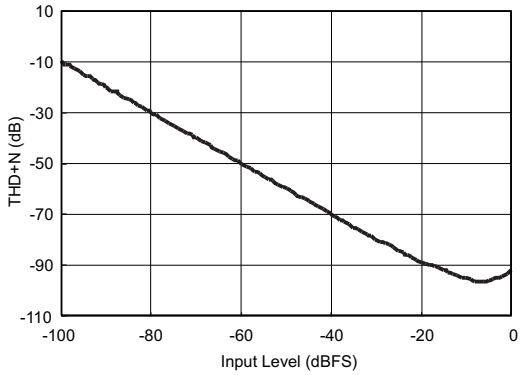


Figure 4. 2 THD+N versus Input Level

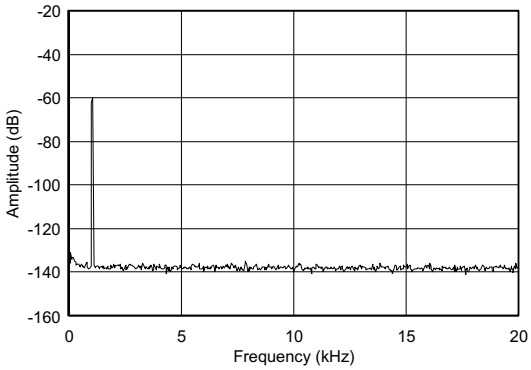


Figure 5. 1 FFT Plot At -60db Input

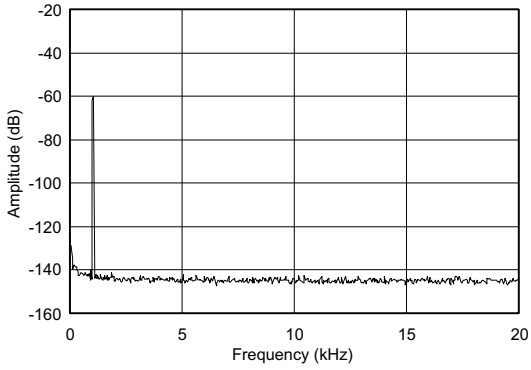


Figure 6. 2 FFT Plot At -60db Input

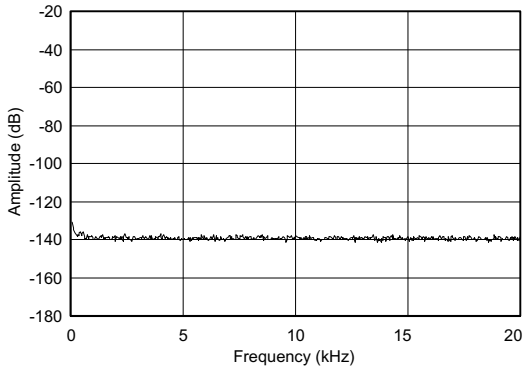


Figure 7. 1 FFT Plot At Bipolar Zero Data (BPZ)

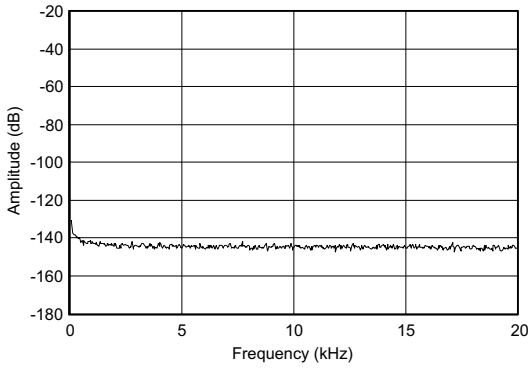


Figure 8. 2 FFT Plot at BPZ

Typical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

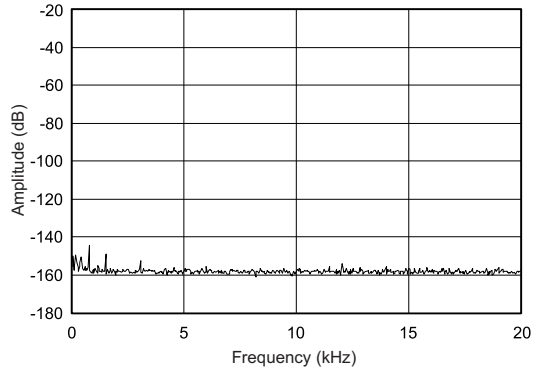


Figure 9. 1 FFT Plot at BPZ With Analog Mute (Amute)

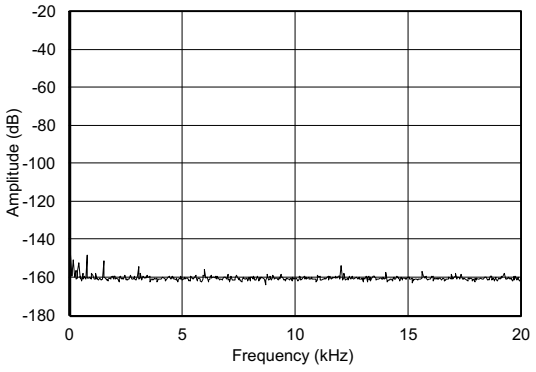


Figure 10. 2 FFT Plot at BPZ With Amute

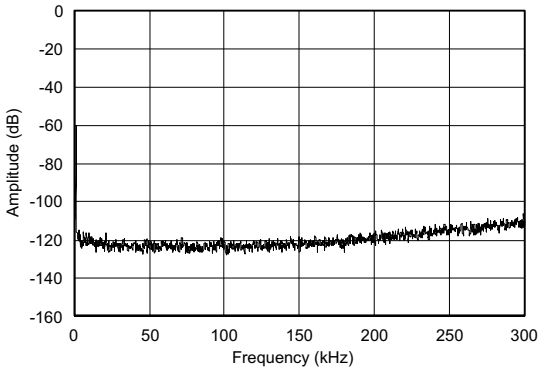


Figure 11. 1 FFT Plot at -60dB to 300khz

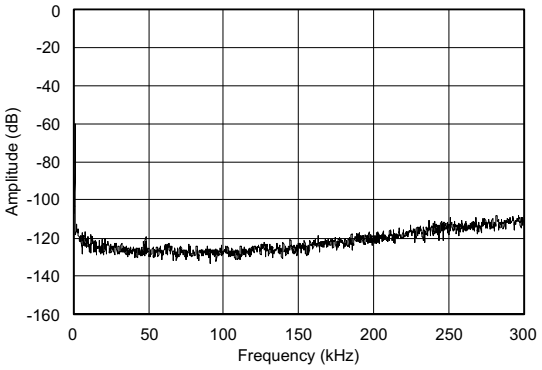


Figure 12. 2 FFT Plot at -60dB to 300khz

9 Detailed Description

9.1 Overview

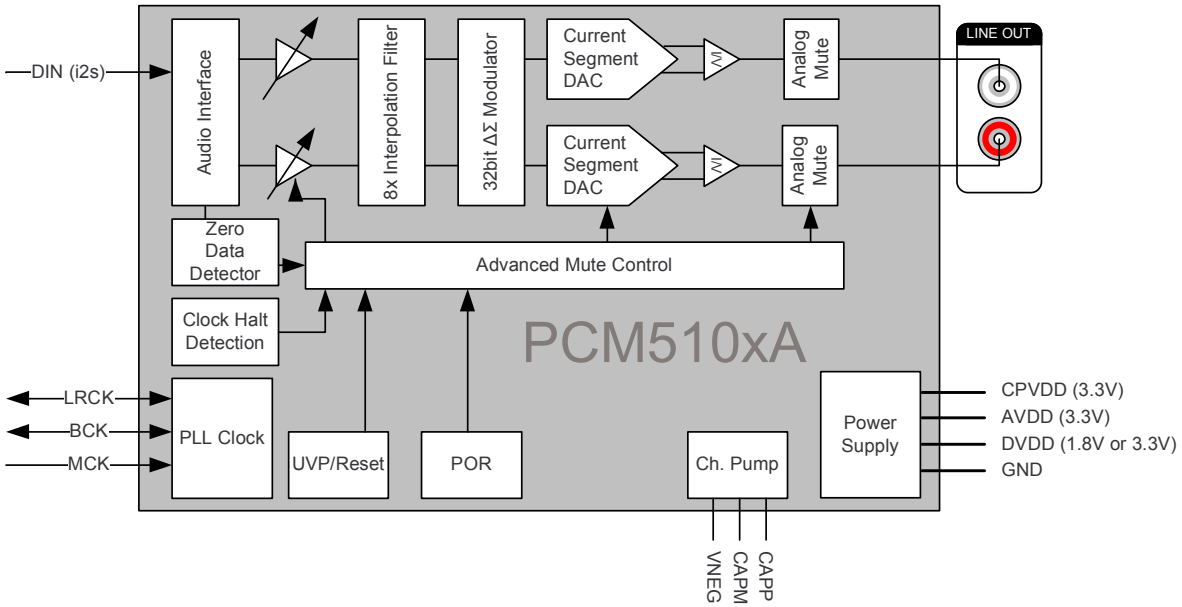
The integrated PLL on the device provided adds the flexibility to remove the system clock (commonly known as master clock), allowing a 3-wire I^2S connection and reducing system EMI.

Powersense undervoltage protection utilizes a two-level mute system. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data), then mutes the analog circuit.

Compared with existing DAC technology, the PCM510xA offers up to 20dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100kHz OBN measurements all the way to 3MHz).

The PCM510xA accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384kHz are supported.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Terminology

Sampling frequency is symbolized by "f_S". Full scale is symbolized by "FS". Sample time as a unit is symbolized by "t_S".

Feature Description (continued)

9.3.2 Audio Data Interface

9.3.2.1 Audio Serial Interface

The audio interface port is a 3-wire serial port with the signals LRCK, BCK, and DIN. BCK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM510xA on the rising edge of BCK. LRCK is the serial audio left/right word clock. LRCK polarity for Left/Right is given by the format selected.

Table 1. PCM510xA Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f_S]	SCK RATE [x f_S]	BCK RATE [x f_S]
Hardware Control	I^2S/LJ	32, 24, 20, 16	Up to 192kHz	128 – 3072 (≤50MHz)	64, 48, 32
			384kHz	64, 128	64, 48, 32

The PCM510xA requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than 4 LRCK periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and BCK is completed.

9.3.2.2 PCM Audio Data Formats

The PCM510xA supports industry-standard audio data formats, including standard I^{2}S and left-justified. Data formats are selected using the FMT (pin 16), Low for I^{2}S, and High for Left-justified. All formats require binary 2s-complement, MSB-first audio data; up to 32-bit audio data is accepted.

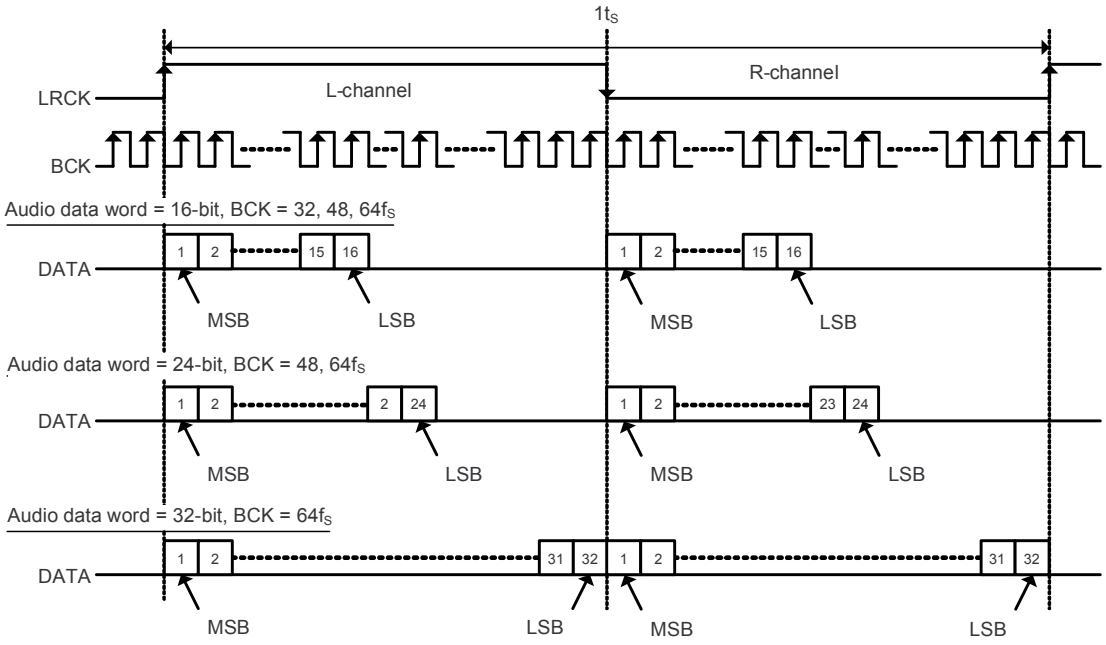
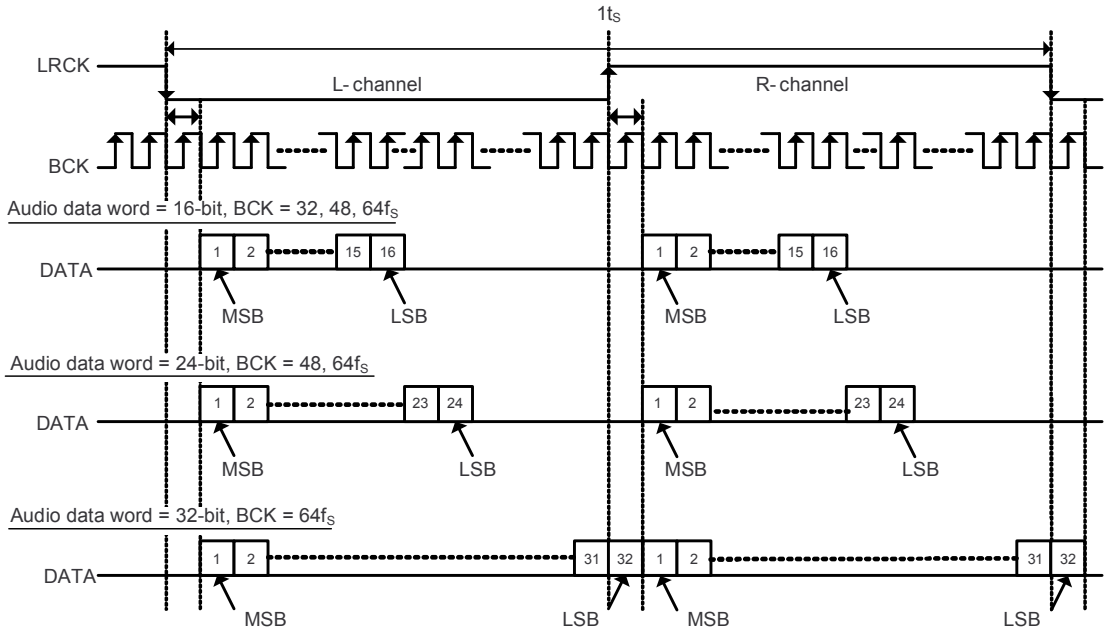


Figure 13. Left Justified Audio Data Format



I^{2}S Data Format; L-channel = LOW, R-channel = HIGH

Figure 14. I^{2}S Audio Data Format

9.3.2.3 Zero Data Detect

The PCM510xA has a zero-data detect function. When the device detects continuous zero data, it enters a full analog mute condition. The PCM510xA counts zero data over 1024 LRCKs (21ms @ 48kHz) before setting analog mute.

In Hardware mode, the device uses default values.

9.3.3 XSMT Pin (Soft Mute / Soft Un-Mute)

An external digital host controls the PCM510xA soft mute function by driving the XSMT pin with a specific minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM510xA requires t_r and t_f times of less than 20ns. In the majority of applications, this is no problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3V to 0V), a soft digital attenuation ramp begins. -1dB attenuation is then applied every sample time from 0dBFS to - ∞. The soft attenuation ramp takes 104 samples.

When the XSMT pin is shifted from low to high (0V to 3.3V), a soft digital “un-mute” is started. 1dB gain steps are applied every sample time from - ∞ to 0dBFS. The un-mute takes 104 samples.

In systems where XSMT is not required, it can be directly connected to AVDD.

9.3.4 Audio Processing

9.3.4.1 Interpolation Filter

The PCM510xA provides 2 types of interpolation filter. Users can select which filter to use by using the FLT pin (pin11)

Table 2. Digital Interpolation Filter Options

FLT Pin	Description
0	FIR Normal x8/x4/x2/x1 Interpolation Filters
1	IIR Low Latency x8/x4/x2/x1 Interpolation Filters

The Normal x8/x4/x2/x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 3. Normal x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22t_S$		s

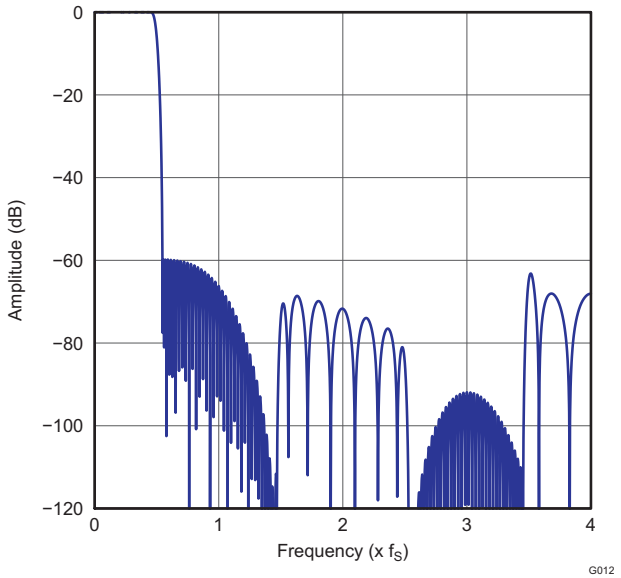


Figure 15. Normal x8 Interpolation Filter Frequency Response

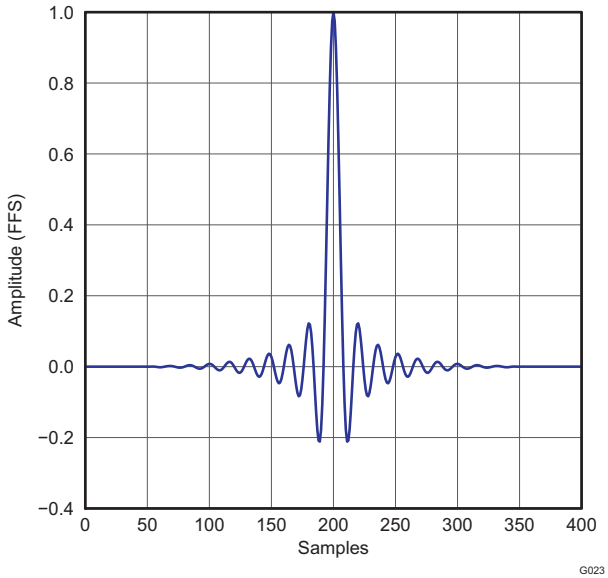


Figure 16. Normal x8 Interpolation Filter Impulse Response

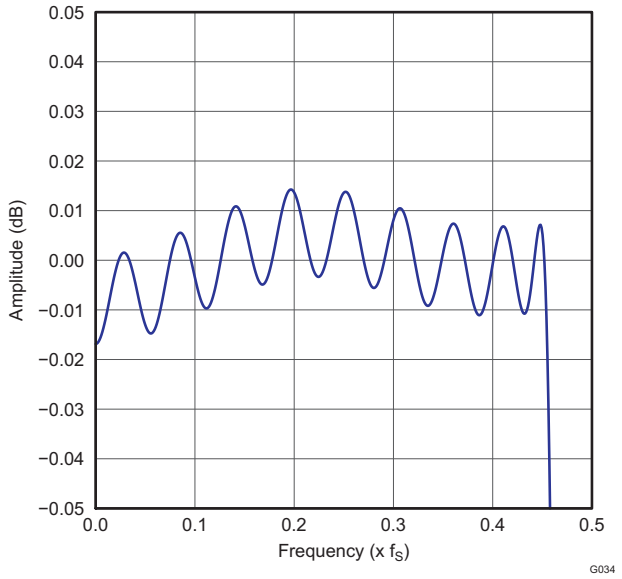


Figure 17. Normal x8 Interpolation Filter Passband Ripple

The Normal x4/x2/x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 4. Normal x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22t_S$		s

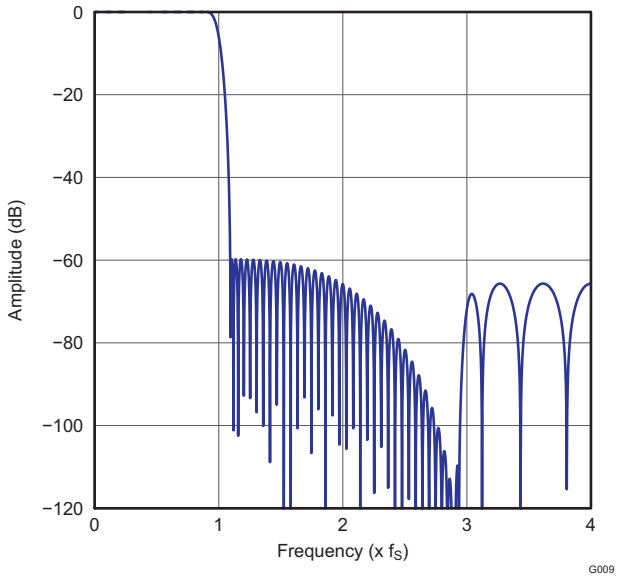


Figure 18. Normal x4 Interpolation Filter Frequency Response

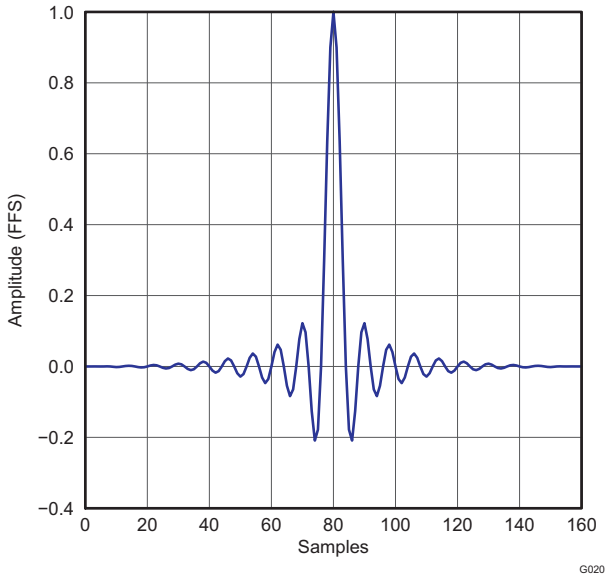


Figure 19. Normal x4 Interpolation Filter Impulse Response

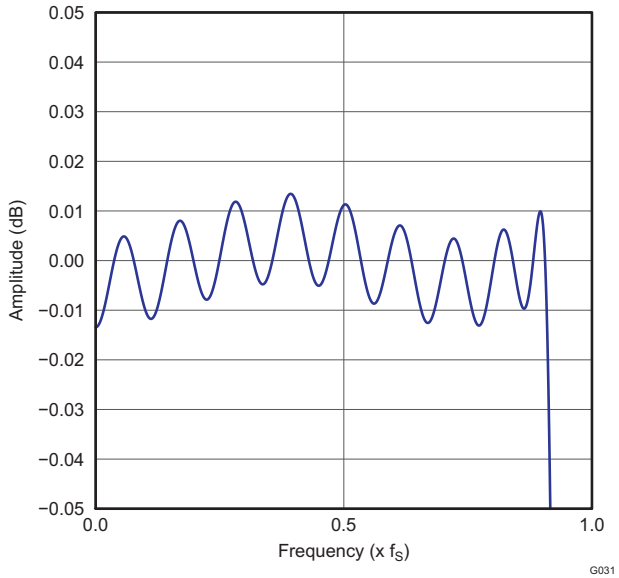


Figure 20. Normal x4 Interpolation Filter Passband Ripple

Normal x2 / x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 5. Normal x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22t_S$		s

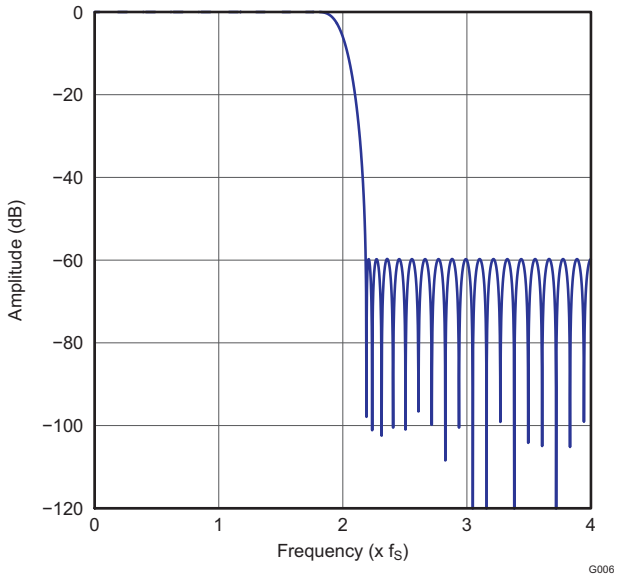


Figure 21. Normal x2 Interpolation Filter Frequency Response

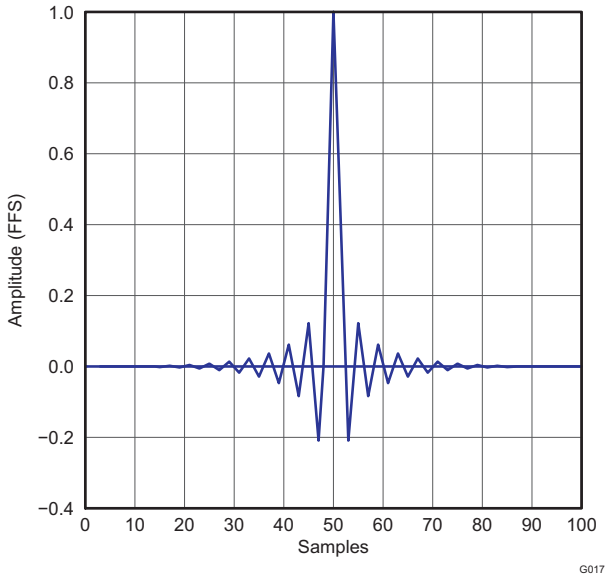


Figure 22. Normal x2 Interpolation Filter Impulse Response

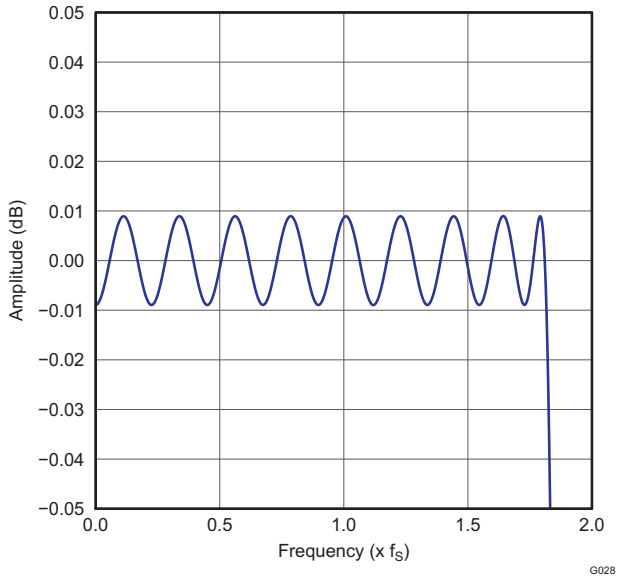


Figure 23. Normal x2 Interpolation Filter Passband Ripple

The low-latency x8 / x4 / x2 / x1(bypass) Interpolation filter is programmed in 256 cycles 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 6. Low latency x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–52	dB
Filter Group Delay		$3.5t_S$	s

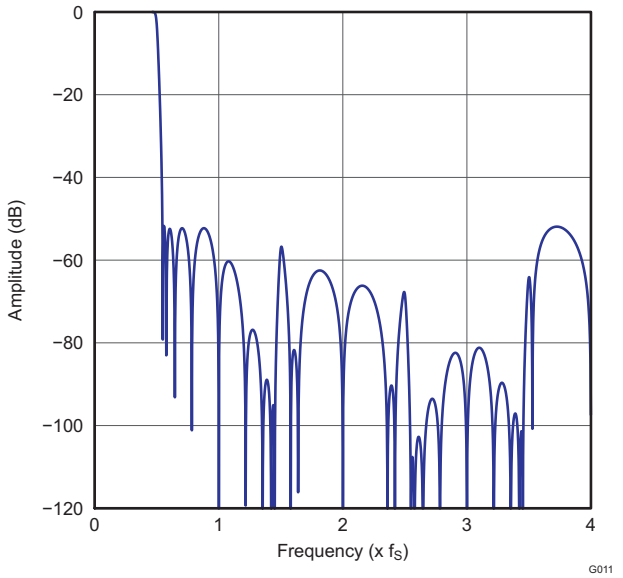


Figure 24. Low latency x8 Interpolation Filter Frequency Response

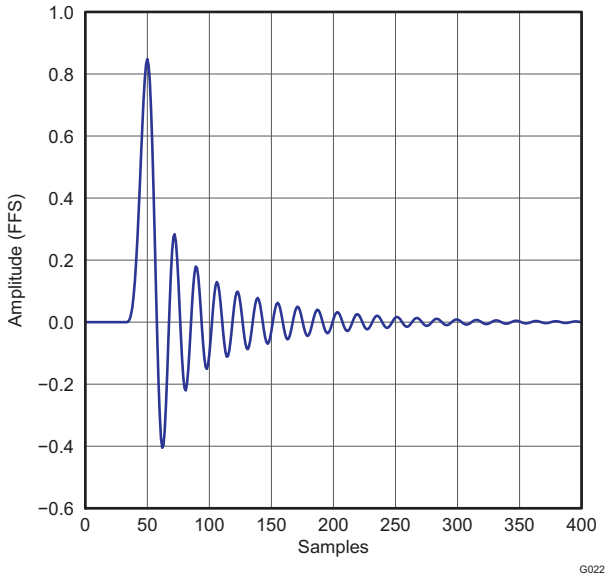


Figure 25. Low latency x8 Interpolation Filter Impulse Response

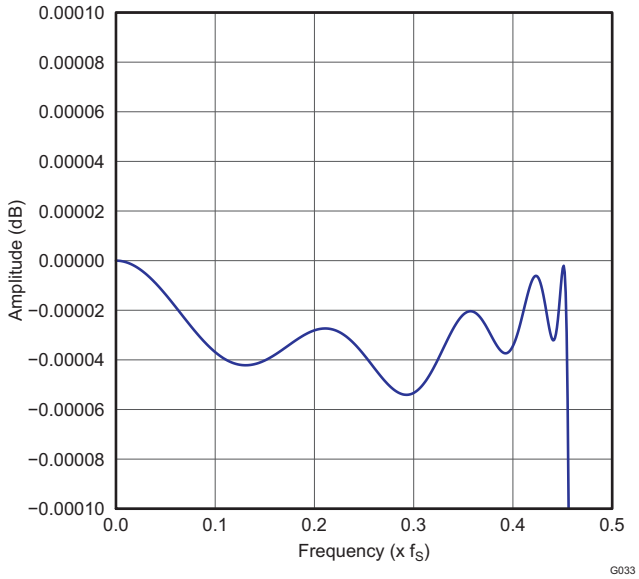


Figure 26. Low latency x8 Interpolation Filter Passband Ripple

Table 7. Low latency x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $3.455f_S$	–52	dB
Filter Group Delay		$3.5t_S$	s

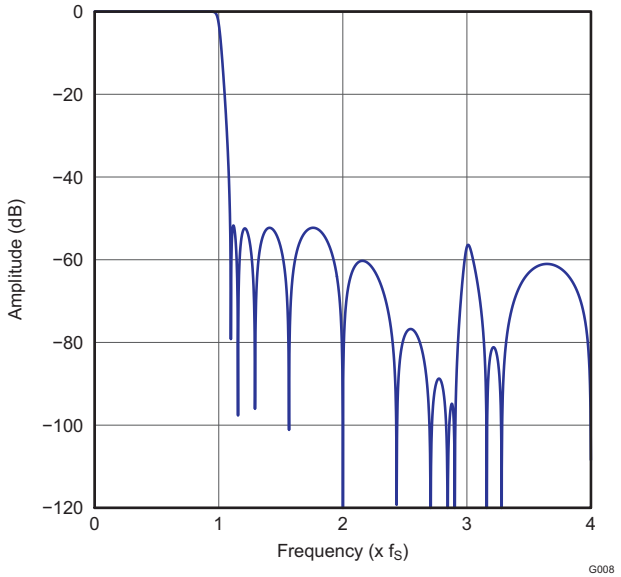


Figure 27. Low latency x4 Interpolation Filter Frequency Response

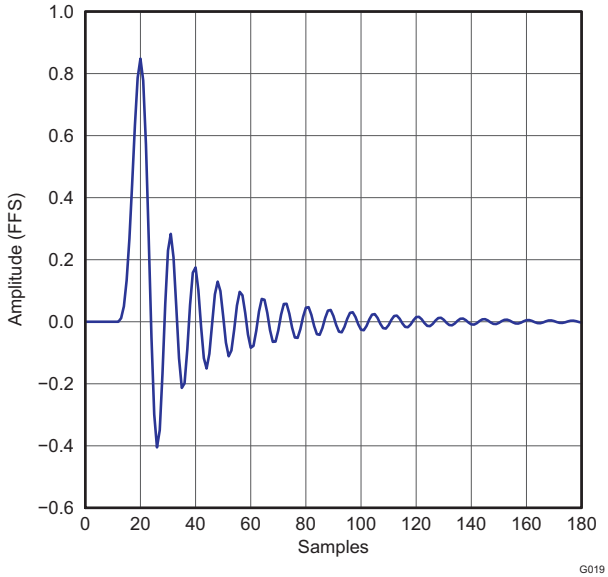


Figure 28. Low latency x4 Interpolation Filter Impulse Response

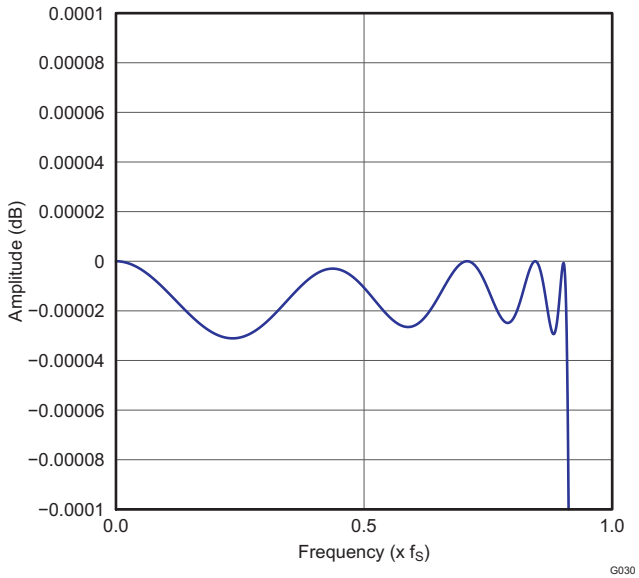


Figure 29. Low latency x4 Interpolation Filter Passband Ripple

Table 8. Low latency x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $1.455f_S$	–52	dB
Filter Group Delay		$3.5t_S$	s

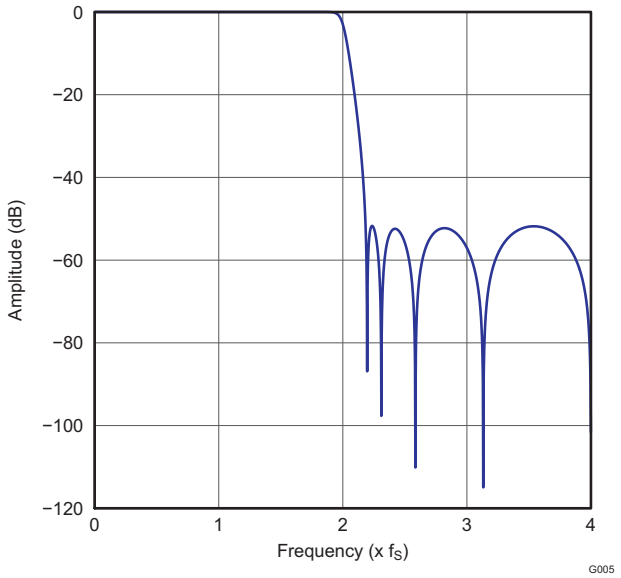


Figure 30. Low latency x2 Interpolation Filter Frequency Response

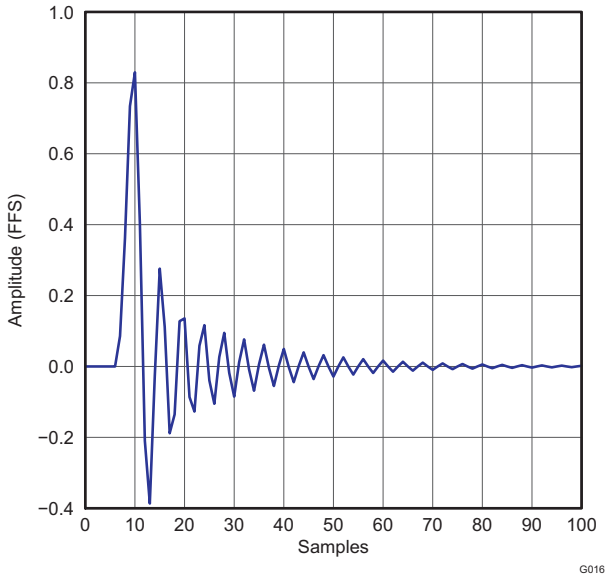


Figure 31. Low latency x2 Interpolation Filter Impulse Response

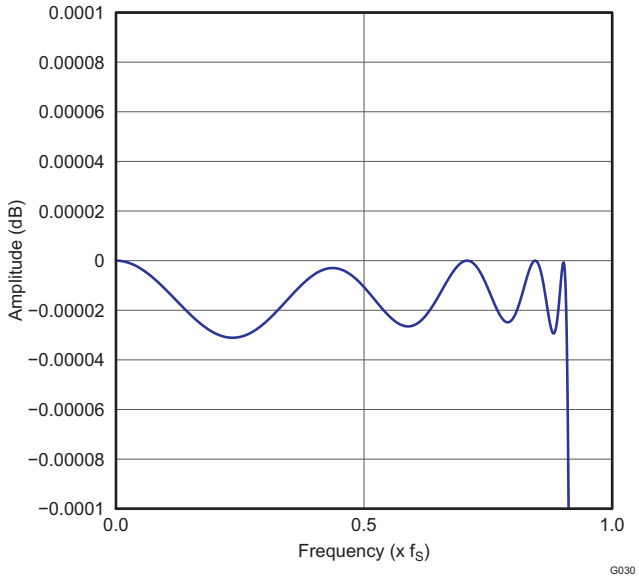


Figure 32. Low latency x2 Interpolation Filter Passband Ripple

9.3.5 Reset and System Clock Functions

9.3.5.1 Clocking Overview

The PCM510xA devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface in one form or another.

The data flows at the sample rate (f_S). Once the data is brought into the serial audio interface, it gets processed, interpolated and modulated all the way to 128 × f_S before arriving at the current segments for the final digital to analog conversion.

The Serial Audio Interface typically has 4 connections SCK (System Master Clock), BCK (Bit Clock), LRCK (Left Right Word Clock) and Data. The device has an internal PLL that is used to take either SCK or BCK and create the higher rate clocks required by the and the DAC clock.

9.3.5.2 Clock Slave Mode With Master Clock (SCK) Input (4 Wire I^2S)

The PCM510xA requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input and supports up to 50MHz. The PCM510xA system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 8kHz, 16kHz, (32kHz - 44.1kHz - 48kHz), (88.2kHz - 96kHz), (176.4kHz -192kHz), and 384kHz with ±4% tolerance are supported. **Values in the parenthises are "grouped" when detected, e.g. 88.2kHZ and 96kHz are detected as "double rate", 32kHz, 44.1kHz and 48kHz will be detected as "single rate".**

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 9 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1MHz and 50MHz, are only supported in software mode, available only in the PCM512x, PCM514x, and PCM5242 devices, by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12MHz to generate 44.1kHz (LRCK) and 2.8224MHz (BCK)).

Table 9. System Master Clock Inputs for Audio Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1024 f_S	1152 f_S	1536 f_S	2048 f_S	3072 f_S
8 kHz	–(1)	1.0240(2)	1.5360(2)	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	–(1)	2.0480(2)	3.0720(2)	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	–(1)	4.0960(2)	6.1440(2)	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	–(1)	–(1)
44.1 kHz	–(1)	5.6488(2)	8.4672(2)	11.2896	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)
48 kHz	–(1)	6.1440(2)	9.2160(2)	12.2880	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)
88.2 kHz	–(1)	11.2896(2)	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
96 kHz	–(1)	12.2880(2)	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
176.4 kHz	–(1)	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
192 kHz	–(1)	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
384 kHz	24.5760	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.

See for clock timing requirements.

9.3.5.3 Clock Slave Mode with BCK PLL to Generate Internal Clocks (3-Wire PCM)

The system clock PLL mode allows designers to use a simple 3-wire I^2S audio source. The 3-wire source reduces the need for a high frequency SCK, making PCB layout easier, and reduces high frequency electromagnetic interference.

The internal PLL is disabled as soon as an external SCK is supplied.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. Specific BCK rates are required to generate an appropriate master clock. Table 10 describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

Table 10. BCK Rates (MHz) by LRCK Sample Rate for PCM510xA PLL Operation

	BCK (f_S)	
Sample f (kHz)	**32**	**64**
8	-	-
16	-	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

9.4 Device Functional Modes

9.4.1 External SCK and PLL Activation

As discussed in *Clock Slave Mode with BCK PLL to Generate Internal Clocks (3-Wire PCM)*, the PCM510xA internal PLL supplies a SCK if an external SCK is not present at powerup.

9.4.1.1 Interpolation Filter Modes

Interpolation-filter options are controlled by the FLT pin. See Table 2.

9.4.1.2 44.1kHz De-emphasis

De-emphasis control for 44.1kHz f_S is controlled by the DEMP pin. See *Pin Configuration and Functions*.

9.4.1.3 Audio Format

Audio format is selected by the FMT pin. See *Pin Configuration and Functions*.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Typical Applications

10.1.1.1 Hardware Controlled DAC Application

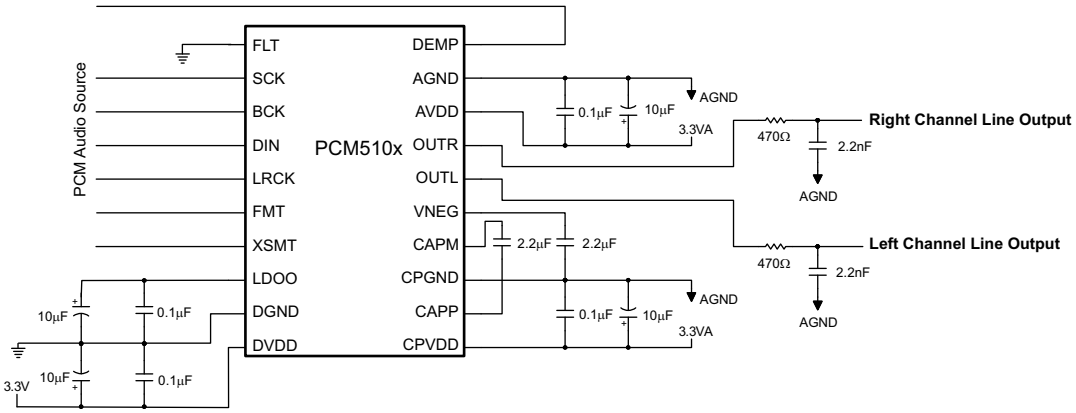


Figure 33. Simplified Schematic, Hardware-Controlled Subsystem

10.1.1.1.1 Example Design Requirements

- Device control method: Hardware control
  - Normal filter latency
  - I2S Digital Audio Interface
  - Power Rail Monitoring from 12V rail
- Single-ended 2.1V_{RMS} analog outputs
- 3 wire I2S interface (BCK PLL)
- Single 3.3V supply

10.1.1.1.2 Detailed Design Procedure

- Device control method: See *Pin Configuration and Functions* and Table 2.
  - Normal filter latency: FLT pin tied low.
  - Audio format selection : FMT pin tied low
- Clock and PLL setup (See *Reset and System Clock Functions*). Ensure incoming BCK meets minimum requirements.
- XSMT pin setup for 12V monitoring.(See *External Power Sense Undervoltage Protection mode (supported only when DVDD = 3.3V)*)
- Single-supply 3.3V operation (See *Setting Digital Power Supplies and I/O Voltage Rails*)
  - LDO

Application Information (continued)

10.1.1.1.3 Application Curve

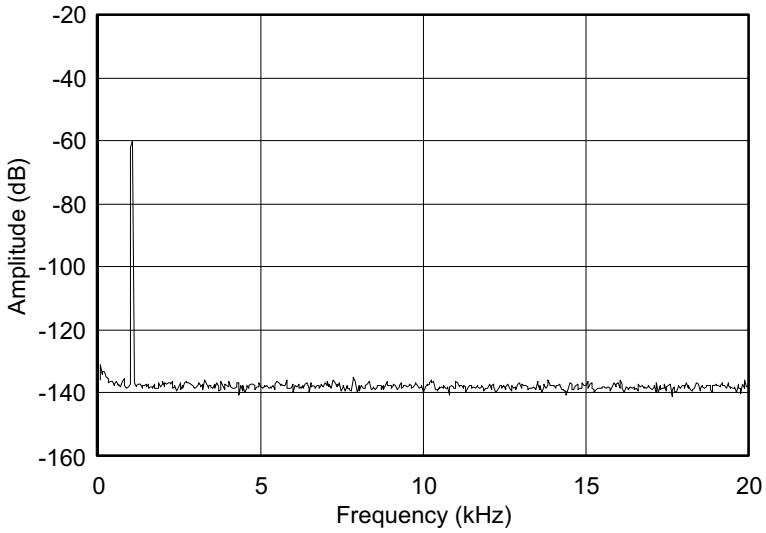


Figure 34. 1 FFT Plot At -60db Input

11 Power Supply Recommendations

11.1 Power Supply Distribution and Requirements

The PCM510xA is powered through the following pins:

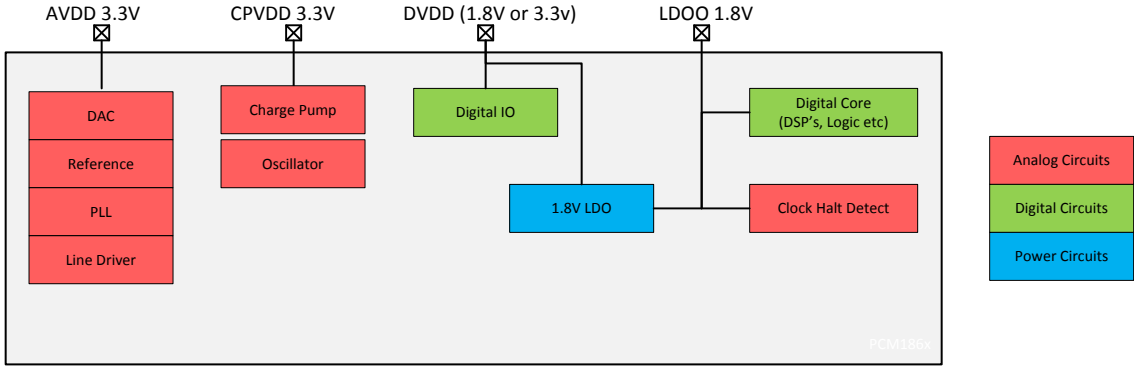


Figure 35. Power Distribution Tree within PCM510xA

Table 11. Power Supply Pin Descriptions

NAME	USAGE / DESCRIPTION
AVDD	Analog Voltage Supply - should be 3.3V. Powers all analog IP that the DAC runs on.
DVDD	Digital Voltage Supply - This is used as the I/O voltage control and the input to the onchip LDO.
CPVDD	Charge Pump Voltage Supply - should be 3.3V
LDOO	Output from the Onchip LDO. Should be used with a 0.1uF decoupling cap. Can be driven (used as power input) with a 1.8V supply to bypass the onchip LDO for lower power consumption.
AGND	Analog Ground
DGND	Digital Ground

11.2 Recommended Powerdown Sequence

Under certain conditions, the PCM510xA can exhibit some pop on power down. Pops are caused by the device not having enough time to detect power loss and start the muting process.

The PCM510xA has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

XSMT = 0

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, closely followed by a hard analog mute. This process takes 150 sample times (t_s) + 0.2mS.

Because this mute time is mainly dominated by the sampling frequency, systems sampling at 192kHz will mute much faster than a 48kHz system.

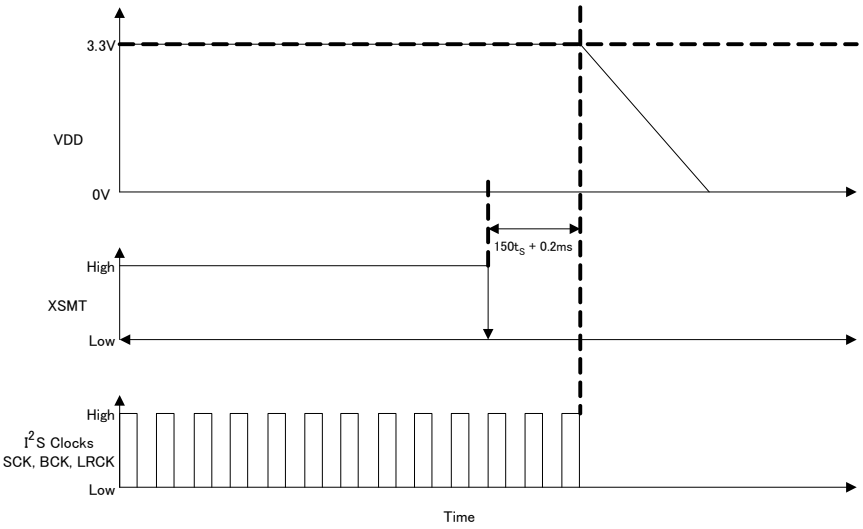
Clock Error Detect

When clock error is detected on the incoming data clock, the PCM510xA switches to an internal oscillator, and continues to the drive the output, while attenuating the data from the last known value. Once this process is complete, the PCM510xA outputs are hard muted to ground.

11.2.1 Planned Shutdown

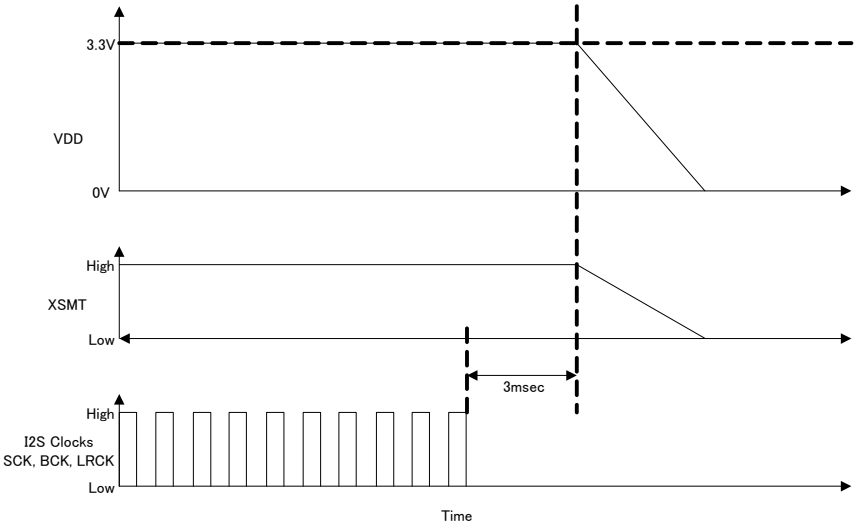
These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways:

1. Assert XSMT low $150t_S$ + 0.2mS before power is removed.



Recommended Powerdown Sequence (continued)

2. Stop I^2S clocks (SCK, BCK, LRCK) 3ms before powerdown as shown below:



11.2.2 Unplanned Shutdown

Many systems use a low-noise regulator to provide an AVDD 3.3V supply for the DAC. The XSMT Pin can take advantage of such a feature to measure the pre-regulated output from the system SMPS to mute the output before the entire SMPS discharges. Figure 36 shows how to configure such a system to use the XSMT pin. The XSMT pin can also be used in parallel with a GPIO pin from the system microcontroller/DSP or Power Supply.

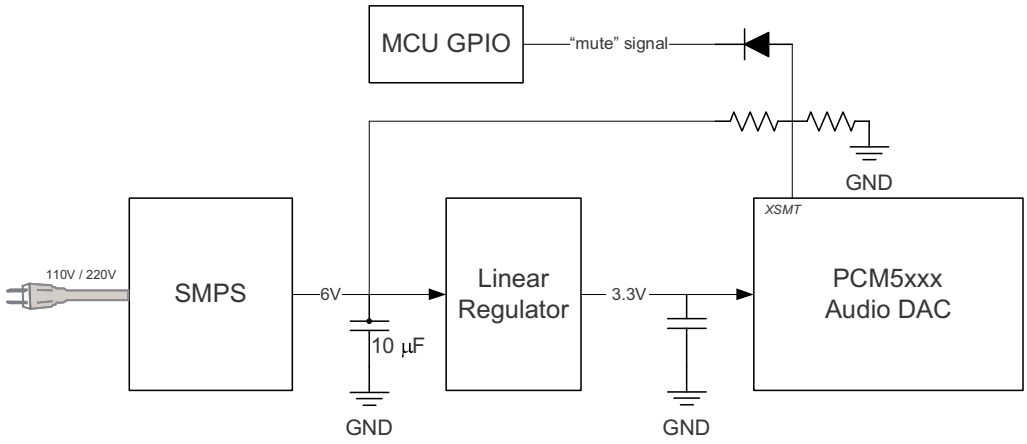


Figure 36. Using the XSMT Pin

11.3 External Power Sense Undervoltage Protection mode (supported only when DVDD = 3.3V)

The XSMT pin can also be used to monitor a system voltage, such as the 24VDC LCD TV backlight, or 12VDC system supply using a voltage divider created with two resistors. (See Figure 37)

- If the XSMT pin makes a transition from “1” to “0” over 6ms or more, the device switches into external under-voltage protection mode. This mode uses two trigger levels.
- When the XSMT pin level reaches 2V, soft mute process begins.
- When the XSMT pin level reaches 1.2V, analog mute engages, regardless of digital audio level, and analog shutdown begins. (DAC and related circuitry powers down).

A timing diagram to show this is shown in Figure 38.

NOTE

The XSMT input pin voltage range is from -0.3V to DVDD + 0.3V.The ratio of external resistors must produce a voltage within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the XSMT pin higher than DVDD+0.3V.

For example, if the PCM510xA is monitoring a 12V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions is 3V. A voltage spike higher than 14.4V causes a voltage greater than 3.6V (DVDD+0.3) on the XSMT pin, potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.

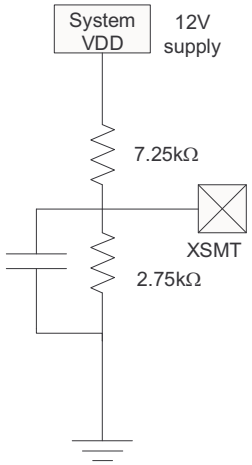


Figure 37. XSMT in External UVP Mode

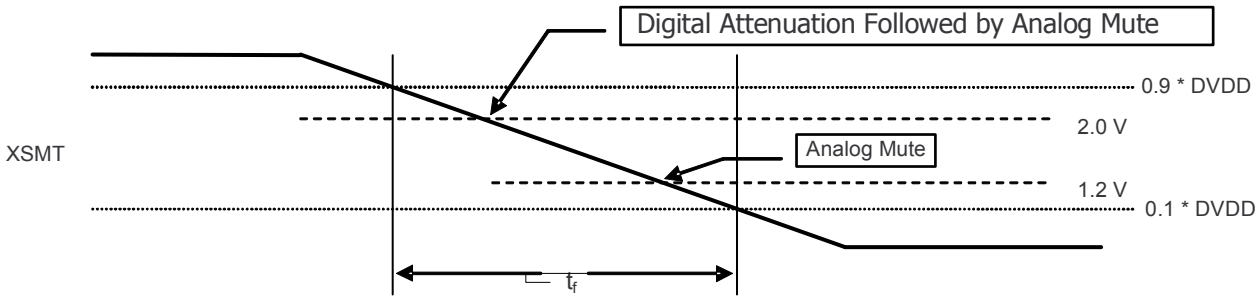


Figure 38. XSMT Timing for Undervoltage Protection

11.4 Power-On Reset Function

Power-On Reset, DVDD 3.3V Supply

The PCM510xA includes a power-on reset function shown in Figure 39. With V_{DD} > 2.8V, the power-on reset function is enabled. After the initialization period, the PCM510xA is set to its default reset state.

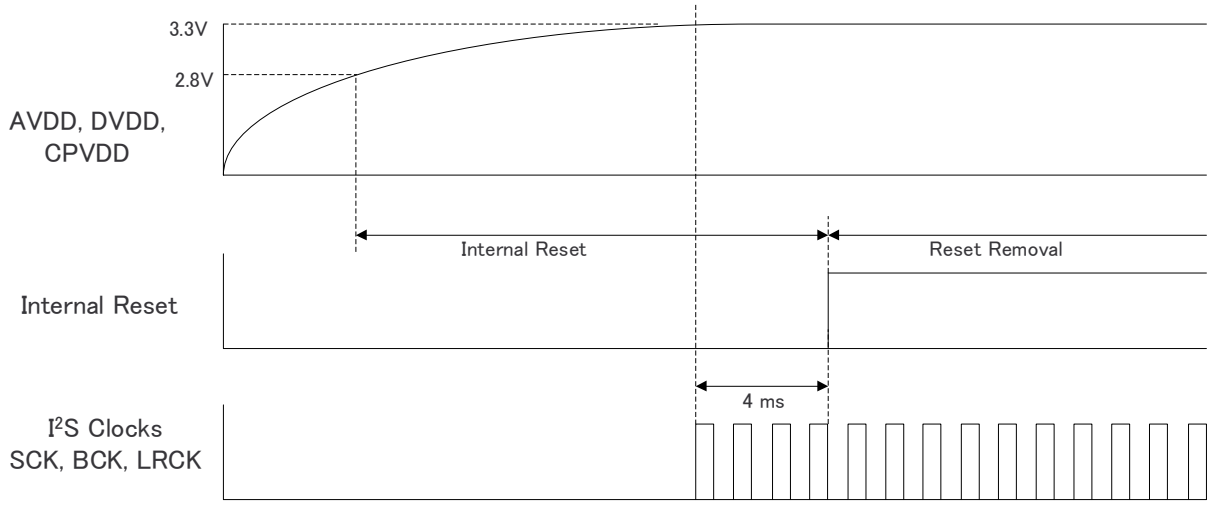


Figure 39. Power-On Reset Timing, DVDD = 3.3V

Power-On Reset Function (continued)

Power-On Reset, DVDD 1.8V Supply

The PCM510xA includes a power-on reset function shown in Figure 40 operating at DVDD=1.8V. With AVDD greater than approximately 2.8V, CPVDD greater than approximately 2.8V, and DVDD greater than approximately 1.5V, the power-on reset function is enabled. After the initialization period, the PCM510xA is set to its default reset state.

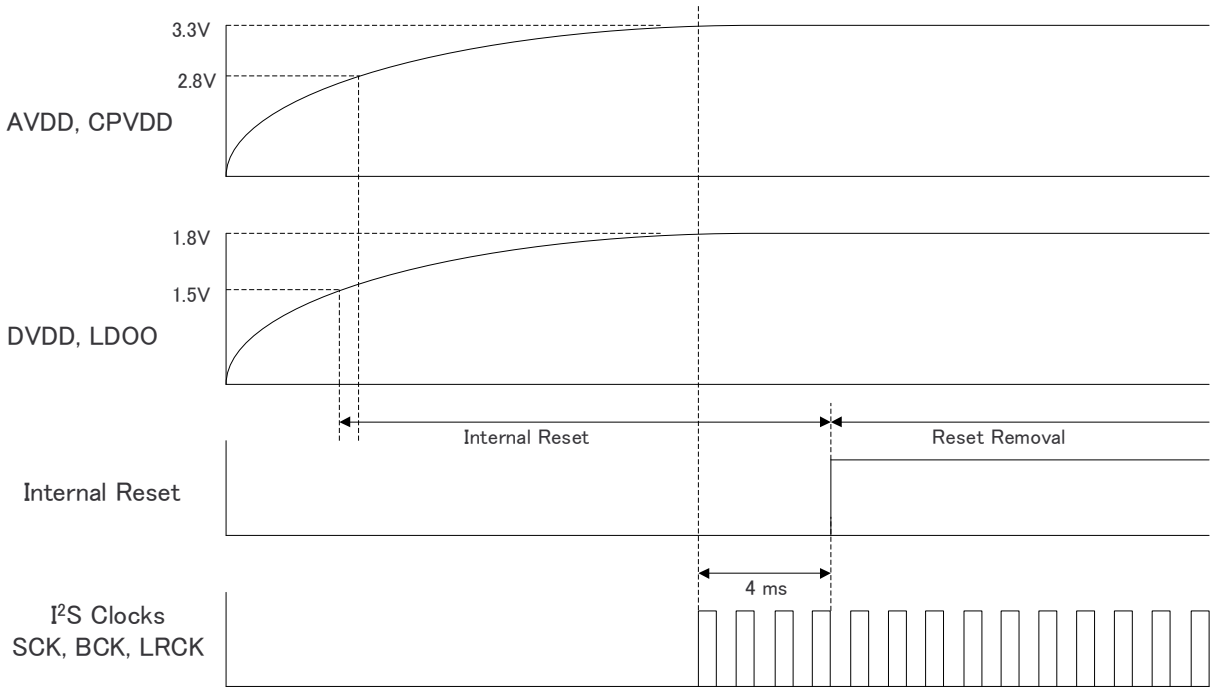


Figure 40. Power-On Reset Timing, DVDD = 1.8V

11.5 PCM510xA Power Modes

11.5.1 Setting Digital Power Supplies and I/O Voltage Rails

The internal digital core of the PCM510xA runs from a 1.8V supply. This can be generated by the internal LDO, or by an external 1.8V supply.

DVDD is used to set the I/O voltage, and to be used as the input to the onchip LDO that creates the 1.8V required by the digital core.

For systems that require 3.3V IO support, but lower power consumption, DVDD should be connected to 3.3V and LDOO can be connected to an external 1.8V source. Doing so will disable the onchip LDO.

When setting IO voltage to be 1.8V, both DVDD and LDOO must be provided with an external 1.8V supply.

11.5.2 Power Save Modes

The PCM510xA offers two power-save modes; standby and power-down.

When a clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM510xA automatically enters standby mode. The DAC and line driver are also powered down. The device can also be placed in standby mode via software command.

When BCK and LRCK remain at a low level for more than 1 second, the PCM510xA automatically enters power-down mode. Power-down mode disables the negative charge pump and bias/reference circuit, in addition to those disabled in standby mode. The device can also be placed in power-down mode via software command.

When expected Audio clocks (SCK, BCK, LRCK) are applied to the PCM510xA, the device starts its powerup sequence automatically.

12 Layout

12.1 Layout Guidelines

- The PCM510xA is a simple device to layout. Most engineers use a shared common ground for the entire device. GND can be consider AGND and DGND connected.
- Good system partitioning should keep digital clock and interface traces away from the differential analog outputs for highest analog performance. This reduces any high speed clock return currents influencing the analog outputs.
- Power supply and charge pump decoupling capacitors should be placed as close as possible to the device.
- The thermal pad on the underside of the package should be connected to GND.
- The top layer should be used for routing signals, whilst the bottom layer can be used for GND.

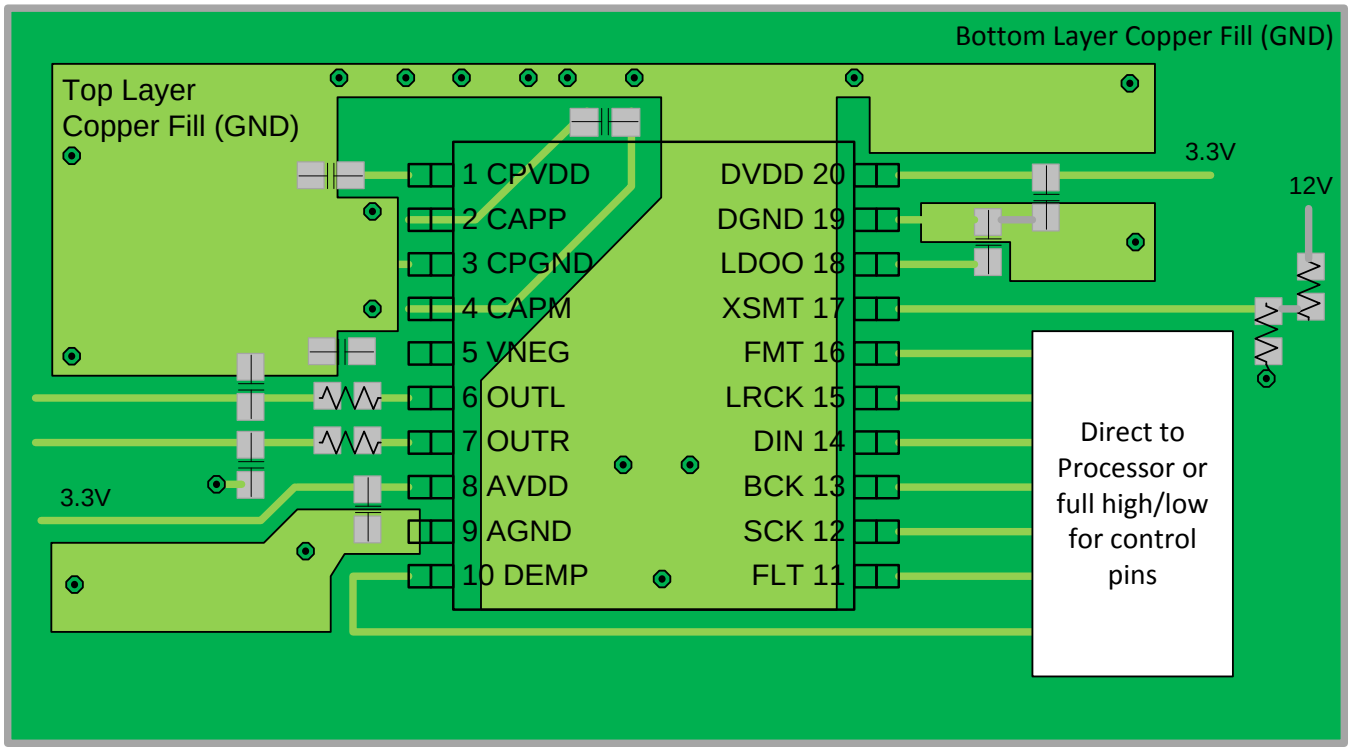


Figure 41. PCM510x Layout Example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
PCM5100A	Click here	Click here	Click here	Click here	Click here
PCM5101A	Click here	Click here	Click here	Click here	Click here
PCM5102A	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

E2E™ Audio Converters Forum TI

E2E Community

13.3 Trademarks

System Two Cascade, Audio Precision are trademarks of Audio Precision.
DirectPath, Directpath are trademarks of Texas, Instruments, Inc..
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

14.1 Mechanical Data

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM5100APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5100A	Samples
PCM5100APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5100A	Samples
PCM5100AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	P5100AQ1	Samples
PCM5101APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5101A	Samples
PCM5101APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5101A	Samples
PCM5101AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	P5101AQ1	Samples
PCM5102APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5102A	Samples
PCM5102APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5102A	Samples
PCM5102AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	P5102AQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF PCM5100A, PCM5100A-Q1, PCM5101A, PCM5101A-Q1, PCM5102A, PCM5102A-Q1 :

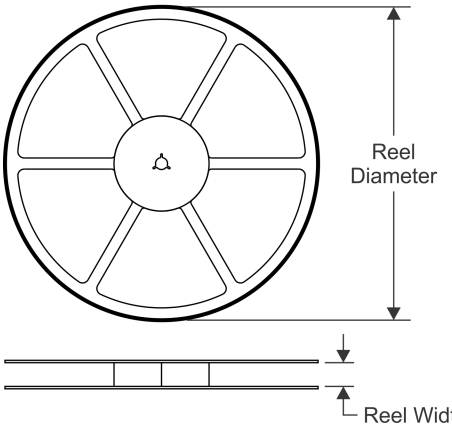
- Catalog: PCM5100A, PCM5101A, PCM5102A
- Automotive: PCM5100A-Q1, PCM5101A-Q1, PCM5102A-Q1

NOTE: Qualified Version Definitions:

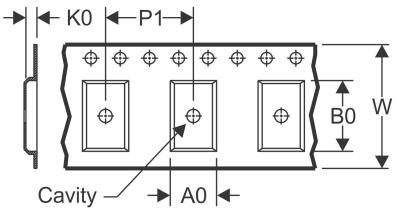
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

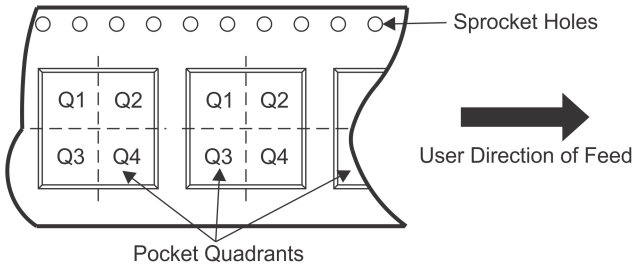


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

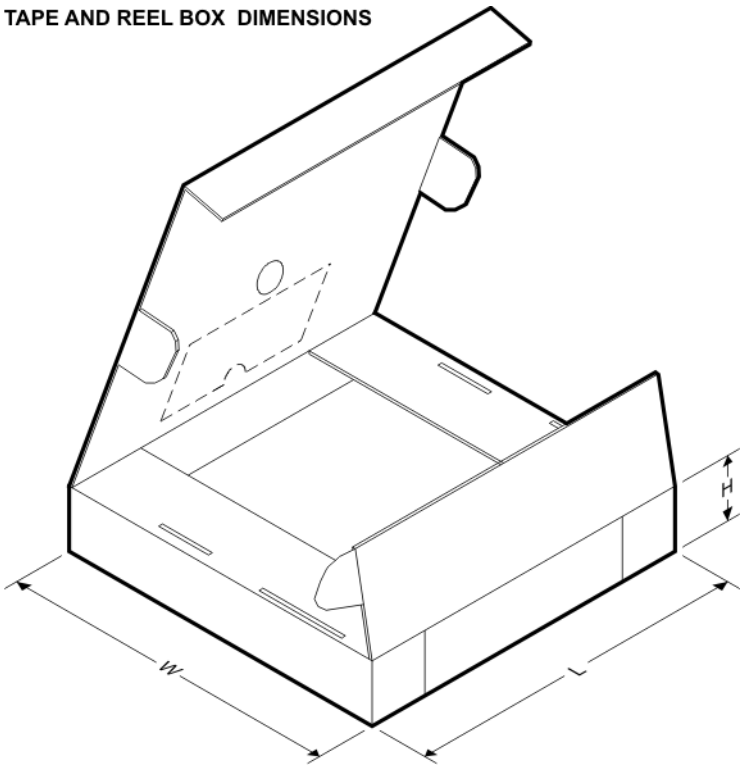
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5100APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5100AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5101APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5101AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5102APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5102AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

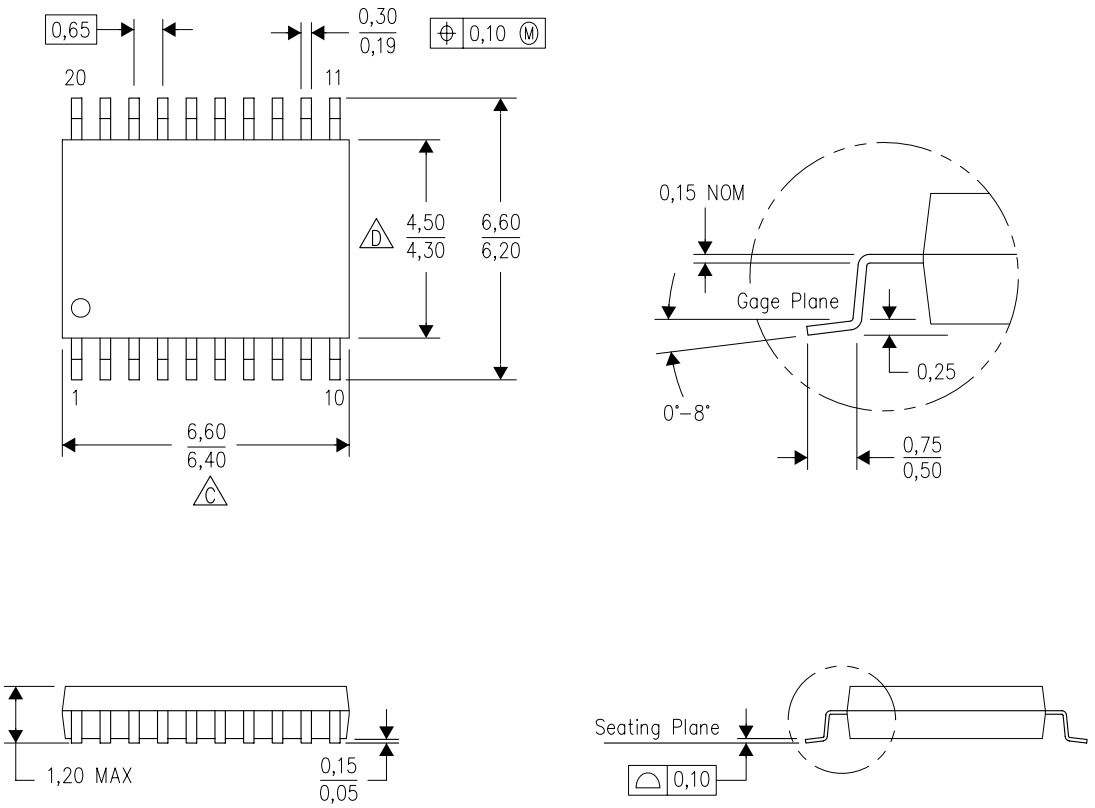
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5100APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PCM5100AQPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0
PCM5101APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PCM5101AQPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0
PCM5102APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PCM5102AQPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

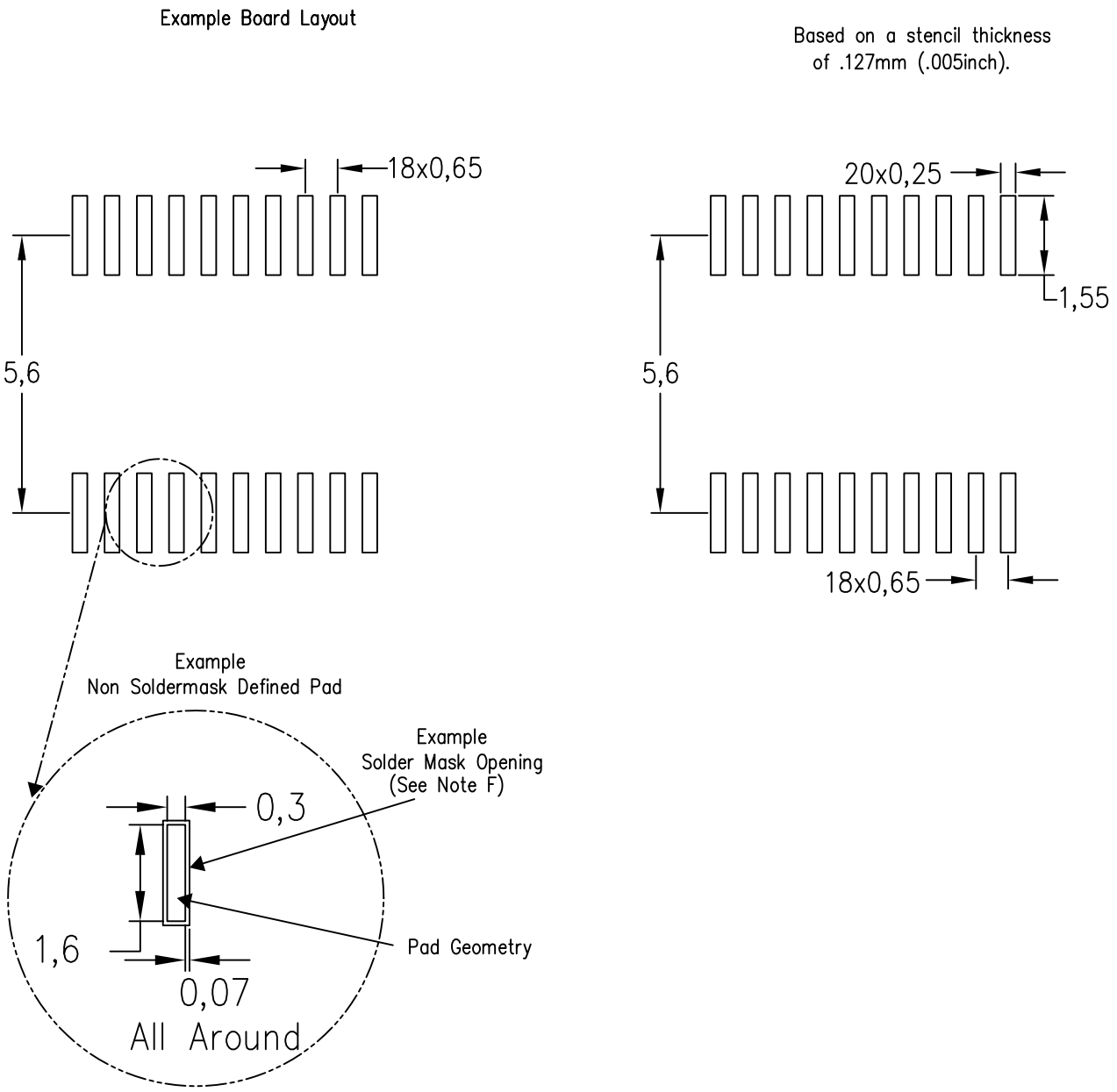
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
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